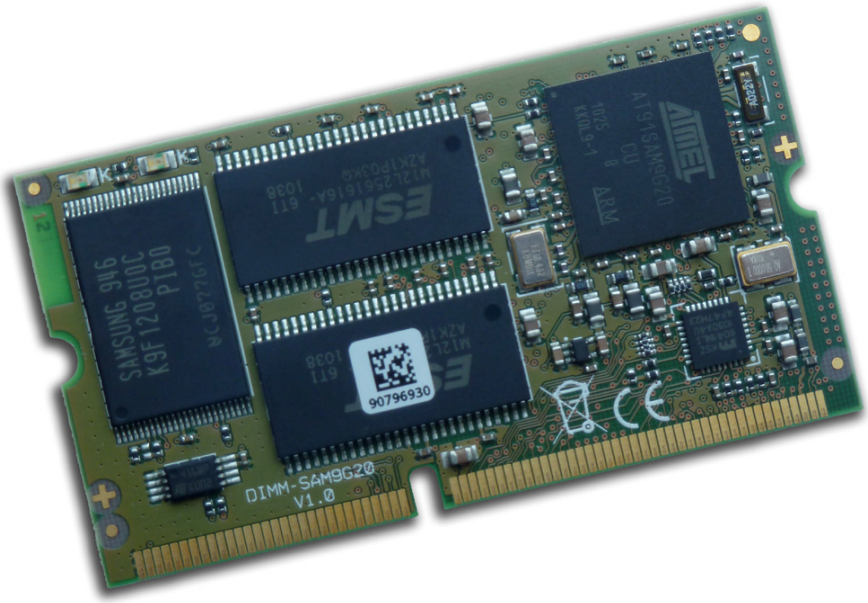

DIMM-SAM9G20

Hardware Manual

Document Revision V1.0

1 Contents

1 Contents 2
2 Pictures 4
3 Tables 5
4 User Information 6
4.1 About This Manual 6
4.2 Copyright 6
4.3 Trademarks 6
4.4 Limited Warranty for Open Source Software 6
4.5 Technical Support 7
5 Introduction 8
5.1 DIMM-SAM9G20 Architecture 8
5.2 Feature Summary 9
5.3 Block Diagram 9
5.4 Functional Description 10
5.4.1 SO-DIMM connector 10
5.4.2 Power supply 10
5.4.3 Memory Layout 10
5.4.4 Ethernet Phy 11
6 DIMM-SAM9G20 Module Pinout 12
7 DIMM-SAM9G20 Peripherals Pin Assignment 14
7.1 USART0 14
7.2 USART1 14
7.3 USART2 14
7.4 USART3 15
7.5 USART4 15
7.6 USART5 15
7.7 MCI 15
7.8 SPI0 16
7.9 SPI1 16
7.10 SSC0 16
7.11 TWI 16
7.12 TC0, TC1, TC2 17
7.13 TC3, TC4, TC5 17
7.14 ADC 17
8 Signal Description 18
8.1 Control Signals 18
8.1.1 nRESET 18
8.1.2 nBOOTMODE 18
8.1.3 VDDBU 18
8.1.4 WKUP 18
8.1.5 SHDN 19
8.1.6 +1.0V 19
8.1.7 Ethernet Signals 19
9 Mechanical Dimensions 20
9.1 DIMM-SAM9G20 Module 20
9.2 DIMM Connector 20
10 Installing the DIMM-SAM9G20 21

10.1 Installing the module 21
11 Technical Specifications 22
12 Important Documents 23
12.1 Atmel AT91SAM9G20 Datasheet 23
12.2 Micrel KSZ80431NL Datasheet 23
12.3 Samsung K9F1208X0C Datasheet 23
12.4 Numonyx P33 Flash Memory Datasheet 23
12.5 ESMT M12L2561616A Datasheet 23
13 Hardware Revision History 24
14 Document Revision History 25

2 Pictures

Module Block Diagram 9
Module Dimensions 20

3 Tables

Module Pinout 13
USART0 Port Pinout 14
USART1 Port Pinout 14
USART2 Port Pinout 14
USART3 Port Pinout 15
USART3 Port Pinout 15
USART3 Port Pinout 15
MCI Port Pinout 15
SPI Port Pinout 16
SPI Port Pinout 16
SSC0 Port Pinout 16
TWI Port Pinout 16
MCI Port Pinout 17
MCI Port Pinout 17
SSC0 Port Pinout 17
DIMM Socket Selection 20

4 User Information

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5 Introduction

5.1 DIMM-SAM9G20 Architecture

The application-specific portion of a standard embedded application typically requires low pin count components such as relays, power supplies and A/D-converters. An embedded Controller requires components of much higher pin-count and higher density circuit boards. The DIMM-SAM9G20 concept separates the high-density circuit board of the embedded Controller from the low density, often two-layer, application-specific baseboard.
To address the drawback of a higher price for an embedded controller-like solution, the DIMM-SAM9G20 performs without discrete peripheral connectors, significantly reducing the cost. In other embedded controller solutions, connectors and their assembly are a significant part of the manufacturing costs. In "low end" solutions, these costs can be as much as 25%. Because the DIMM-SAM9G20 performs without connectors, these costs are significantly decreased and the controller can be integrated on a smaller board surface. The reduction in the number of steps necessary in manufacturing and assembling the component group is another cost-decreasing factor. The one-sided reflow process, as well as exclusion of the wave-solder process, serves to increase the yield in manufacturing and improve quality.
The required SO-DIMM connector is a very inexpensive, standard component and is available from numerous manufacturers. In designing the DIMM-SAM9G20, attention was directed toward its use in embedded applications. Because most peripheral interfaces used in such applications are device-internal (in external interfaces, mainly special customized interfaces are used), the serial interface driver components have been excluded from the DIMM-SAM9G20, leading the interfaces as pure TTL signals to the outside. This further decreases additional costs, while enabling the user to have more flexibility when selecting the interface driver (RS485, RS422, RS232, TTY etc.). The power consumption of the controller architecture is drastically reduced due to the integrated components. This makes the system optimally adaptable with power-saving modes.

The DIMM-SAM9G20 also has minimized or eliminated some of the most critical disadvantages of the microcontroller:

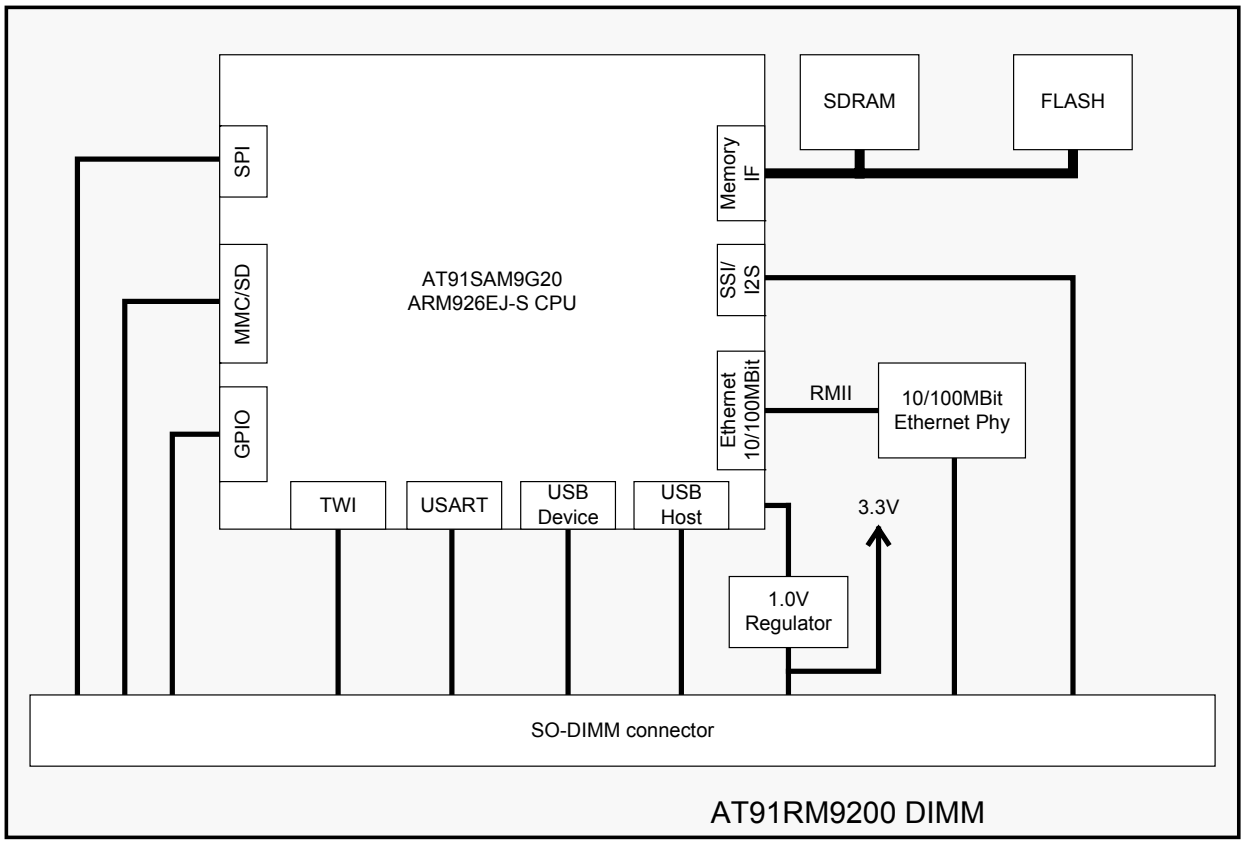
- The DIMM-SAM9G20 today needs less board surface than most micro-controller applications.
- The embedded controller cost has been drastically decreased by the DIMM-SAM9G20.
- The DIMM-SAM9G20 architecture has eliminated the complicated cabling of an embedded PC.

The user receives important advantages by using a DIMM-SAM9G20. Because of the availability of numerous development platforms, the user can begin the software development immediately on any platform with the AT91SAM9G20. This is a factor that may influence the success of a product in today's market, where "time to market" is of high importance. As target hardware becomes available, it can be implemented with no obstacles to operation because it will be unnecessary to change the software. With the SO-DIMM-connector, an exchange for other CPU types is possible, increasing the scalability of the ultimate device. In the case of product information and new designs, the CPU may simply be superseded by a new DIMM-module, saving redesign time. Through continuous development of the DIMM modules, the cost for the life span of a product can be reduced, profiting users.

5.2 Feature Summary

- ATMEL AT91SAM9G20 microcontroller in BGA package with 400 MHz ARM926-EJ-S CPU
- UBOOT GPL boot loader and LINUX operating system
- 64 MB SDRAM memory (optional 128 MB)
- 32-bit SDRAM data bus
- 64 MB NAND FLASH, (larger NAND devices on request)
- alternatively 16 MB NOR Flash memory with 16 bit data bus
- 10 / 100Mbit Ethernet with on board physical layer and fast MII interface
- 6 USART interfaces plus 1 UART
- 2 USB host ports
- 1 USB function port
- 2 MultiMedia Card interfaces
- 1 Two Wire Interface (I^2C)
- 2 LEDs (1 GPIO, 1 ethernet) for status display
- on board 1.0V power supply for processor core voltage
- 144-pins SO-DIMM card edge connector
- ultra small size (67.6 mm x 36.5 mm x 2.5 mm)

5.3 Block Diagram



Picture 1: Module Block Diagram

5.4 Functional Description

5.4.1 SO-DIMM connector

All external connections are accessible through the 144-pins SO-DIMM card edge connector. The following external functionality is available:

- 3V3 power supply input
- 1V0 power supply output (max. 25mW)
- reset_out, reset_in and interrupts
- peripheral interfaces
- JTAG interface and dbg_usart used during production
- 10/100Mbit Ethernet signals

The internal circuitry of the DIMM-SAM9G20 is based on 3V3 low voltage technology. All interface signals are 3V3 only.

5.4.2 Power supply

5.4.2.1 External power supply

The DIMM-SAM9G20 requires an external power supply. You have to power the DIMM-SAM9G20 with a 3V3 / 0,5 A external power supply, connected to the 3V3 pins on the SO-DIMM connector. When using an external power supply, it is strongly advised to place a low ESR capacitor on the carrier board close to the 3V3 input to reduce interference.

5.4.2.2 On board power supply

The core supply voltage for the AT91SAM9G20 is generated on board and is available for reference on the 1V0 pin of the SO-DIMM connector. The power consumption of external components, if any, must be limited to 25mW.

5.4.3 Memory Layout

Equipped with either 512Mbit NAND flash or 128 Mbit Numonyx P33 Flash as well as with two SDRAMs of each 256 Mbit the DIMM-SAM9G20 realizes a total of 64/16 Mbyte Flash and 64 Mbyte SDRAM.

5.4.3.1 Flash

The standard NAND flash memory is accessed using NCS3. The resulting address range is:

64 MByte: 0x4000 0000 - 0x13FF FFFF

The alternative NOR flash memory is accessed using NCS0. The resulting address range is:

16 MByte: 0x1000 0000 - 0x10FF FFFF

5.4.3.2 SDRAM (chip select NCS1)

The SDRAM is accessed with 32 bit data bus width at NCS1. This results in the following address range:

64 MByte: 0x2000 0000 - 0x23FF FFFF

5.4.3.3 Special notes for user reset / watchdog reset usage

The reset controller of the AT91SAM9G20 has a bug which is described in detail in paragraph 44.3.5.1 of the datasheet, rev E.
In order to circumvent this behavior the linux kernel is patched, using an interrupt to terminate the current SDRAM access before executing a reset.
However, this is not 100% secure (the processor may hang without executing the interrupt). If you need 100% security, you have to use an external watchdog circuitry which is able to power cycle the controller module.

5.4.4 Ethernet Phy

A Micrel KSZ8041 is used as physical layer chip. This low-power transceiver for 10/100BASE-TX performs auto negotiation compliant with IEEE 802.3u and auto crossover function. It is specified for the industrial temperature range.
Only the ethernet transformer and connector are externally needed for building up the ethernet interface.
A symmetrical kind of modular jack is needed for auto MDIX functionality. A good choice for a transformer is 'H1102' from Pulse. 'J0024D21' from Pulse can be used as ethernet connector with integrated transformer.
A 1nF / 2kV capacitor should be connected between board ground and chassis ground (which is usually connected to the shield of the RJ45-jack) if not already provided in the magnetic jack.

6 DIMM-SAM9G20 Module Pinout

Pin	Periph_B	Periph_A	GPIO		GPIO	Periph_A	Periph_B	Pin
1	GND				GND			2
3					+3.3V			4
5								6
7								8
9								10
11								12
13								14
15								16
17								18
19								20
21								22
23								24
25								26
27								28
29								30
31								32
33								34
35								36
37								38
39								40
41					nRESET			42
43								44
45								46
47								48
49					VDDBU			50
51					WKUP			52
53	SHDN				PC12	IRQ0	NCS7	54
55		TIOB1	PC7		PA23	TWD		56
57		TWCK	PA24					58
59	nBOOTMODE				GND			60
61	GND				GND			62
63	+3.3V				+3.3V			64
65	MCDB3	SPI0_NPCS0	PA3		+3.3V			66
67	MCCDB	SPI0_MOSI	PA1		PB4	TXD0		68
69		SPI0_SPCK	PA2		TDI			70
71	MCDB0	SPI0_MISO	PA0		PB5	RXD0		72
73	TCK				TDO			74
75	ISI_D7	CTS0	PB27		TMS			76
77	ISI_PCK	RTS1	PB28		PA31	SCK0	TXD4	78
79	SPI0_NPCS1	NCS2	PC11		nTRST			80
81	MCDB1	CTS2	PA5		PB22	DSR0	ISI_D2	82
83	ISI_HSYNC	PCK0	PB30		PC6	TIOB2		84
85		TD0	PB18		PB23	DCD0	ISI_D3	86

Pin	Periph_B	Periph_A	GPIO		GPIO	Periph_A	Periph_B	Pin
87		RD0	PB19		PA4	RTS2	MCDB2	88
89	HDPB				PB12	TXD5	ISI_D10	90
91	HDMB				PB24	DTR0	ISI_D4	92
93	HDPA				PC3		SPI1_NPCS3	94
95	HDMA				PB3	SPI1_NPCS0	TIOA5	96
97	DDP				PB26	RTS0	ISI_D6	98
99	DDM				PC8	NCS4	RTS3	100
101		RF0	PB21		PA10	MCDA2		102
103	TIOA3	SPI1_MISO	PB0		PB13	RXD5	ISI_D11	104
105	TIOB3	SPI1_SPCK	PB2		PB1	SPI1_MOSI	TIOB3	106
107		MCDA3	PA11		PA9	MCDA1		108
109		MCDA0	PA6		PB14	DRXD		110
111		MCCDA	PA7		PA8	MCCK		112
113		TIOA0	PA26		PC5		SPI1_NPCS1	114
115	SCK3		PC0		PC10		CTS3	116
117		TCLK0	PA25		PC9	NCS5	TIOB0	118
119	ISI_MCK	PCK1	PB31		PB9	RXD2		120
121	ISI_D0	RK0	PB20		+1.0V			122
123	ISI_D8	TXD3	PB10		PB11	RXD3	ISI_D9	124
125		TIOA2	PA28		PA29	SCK1		126
127	ISI_D5	RI0	PB25		PB6	TXD1	TCLK1	128
129	GND				PB7	RXD1	TCLK2	130
131		TIOA1	PA27		PA30	SCK2	RXD4	132
133		TXD2	PB8		+3.3V			134
135	ISI_VSYNC	CTS1	PB29		PB17	TF0	TCLK4	136
137		DTXD	PB15		PB16	TK0	TCLK3	138
139	ETH_VDDA				ETH_VDDA			140
141	ETH_RX+				ETH_TX+			142
143	ETH_RX-				ETH_TX-			144

Table 1: Module Pinout

Note: DIMM-SAM9G20 pins 115, 94 can be used as analog inputs AD0 and AD3. The pin is automatically used as analog input if the analog channel is enabled.

7 DIMM-SAM9G20 Peripherals Pin Assignment

Following section describes the pin assignment of the peripheral groups of the AT91SAM9G20 controller available on the DIMM-SAM9G20.

7.1 USART0

Signal	DIMM-Pin	PIO Controller	Port Pin
TXD0	68	PIO B / Peripheral A	PB4
RXD0	72	PIO B / Peripheral A	PB5
nDSR0	82	PIO B / Peripheral A	PB22
nDCD0	86	PIO B / Peripheral A	PB23
nDTR0	92	PIO B / Peripheral A	PB24
RI0	127	PIO B / Peripheral B	PB25
nRTS0	98	PIO B / Peripheral A	PB26
nCTS0	75	PIO B / Peripheral A	PB27
SCLK0	78	PIO A / Peripheral A	PA31

Table 2: USART0 Port Pinout

7.2 USART1

Signal	DIMM-Pin	PIO Controller	Port Pin
TXD1	128	PIO B / Peripheral A	PB6
RXD1	130	PIO B / Peripheral A	PB7
nRTS1	77	PIO B / Peripheral A	PB28
nCTS1	135	PIO B / Peripheral A	PB29
SCLK1	126	PIO A / Peripheral A	PA29

Table 3: USART1 Port Pinout

7.3 USART2

Signal	DIMM-Pin	PIO Controller	Port Pin
TXD2	133	PIO B/ Peripheral A	PB8
RXD2	120	PIO B / Peripheral A	PB9
nRTS2	88	PIO A / Peripheral A	PA4
nCTS2	81	PIO A / Peripheral A	PA5
SCLK2	132	PIO A / Peripheral A	PA30

Table 4: USART2 Port Pinout

7.4 USART3

Signal	DIMM-Pin	PIO Controller	Port Pin
TXD3	123	PIO B / Peripheral A	PB10
RXD3	124	PIO B / Peripheral A	PB11
nRTS3	100	PIO C / Peripheral B	PC8
nCTS3	116	PIO C / Peripheral B	PC10
SCLK3	115	PIO C / Peripheral B	PC0

Table 5: USART3 Port Pinout

7.5 USART4

Signal	DIMM-Pin	PIO Controller	Port Pin
TXD4	78	PIO A / Peripheral B	PA31
RXD4	132	PIO A / Peripheral B	PA30

Table 6: USART4 Port Pinout

7.6 USART5

Signal	DIMM-Pin	PIO Controller	Port Pin
TXD5	78	PIO B / Peripheral A	PB12
RXD5	132	PIO B / Peripheral A	PB13

Table 7: USART5 Port Pinout

7.7 MCI

Signal	DIMM-Pin	PIO Controller	Port Pin
MCCK	112	PIO A / Peripheral A	PA8
MCCDA	111	PIO A / Peripheral A	PA7
MCDA0	109	PIO A / Peripheral A	PA6
MCDA1	108	PIO A / Peripheral A	PA9
MCDA2	102	PIO A / Peripheral A	PA10
MCDA3	107	PIO A / Peripheral A	PA11
MCCDB	127	PIO A / Peripheral B	PA1
MCDB0	71	PIO A / Peripheral B	PA0
MCDB1	81	PIO A / Peripheral B	PA5
MCDB2	88	PIO A / Peripheral B	PA4
MCDB3	65	PIO A / Peripheral B	PA3

Table 8: MCI Port Pinout

7.8 SPI0

Signal	DIMM-Pin	PIO Controller	Port Pin
NPCS0_0	65	PIO A / Peripheral A	PA3
NPCS0_1	79	PIO C / Peripheral B	PC11
MISO0	71	PIO A / Peripheral A	PA0
MOSI0	67	PIO A / Peripheral A	PA1
SPCK0	69	PIO A / Peripheral A	PA2

Table 9: SPI0 Port Pinout

7.9 SPI1

Signal	DIMM-Pin	PIO Controller	Port Pin
NPCS1_0	95	PIO B / Peripheral A	PB3
NPCS1_1	114	PIO C / Peripheral B	PC5
NPCS1_3	94	PIO C/ Peripheral B	PC3
MISO1	71	PIO B / Peripheral A	PB0
MOSI1	67	PIO B / Peripheral A	PB1
SPCK1	69	PIO B / Peripheral A	PB2

Table 10: SPI1 Port Pinout

7.10 SSC0

Signal	DIMM-Pin	PIO Controller	Port Pin
TF0	128	PIO B / Peripheral A	PB17
TK0	130	PIO B / Peripheral A	PB16
TD0	133	PIO B / Peripheral A	PB18
RD0	120	PIO B / Peripheral A	PB19
RK0	123	PIO B / Peripheral A	PB20
RF0	124	PIO B / Peripheral A	PB21

Table 11: SSC0 Port Pinout

7.11 TWI

Signal	DIMM-Pin	PIO Controller	Port Pin
TWD	56	PIO A / Peripheral A	PA23
TWCK	57	PIO A / Peripheral A	PA24

Table 12: TWI Port Pinout

7.12 TC0, TC1, TC2

Signal	DIMM-Pin	PIO Controller	Port Pin
TCLK0	117	PIO A / Peripheral A	PA25
TCLK1	128	PIO B / Peripheral B	PB6
TCLK2	130	PIO B / Peripheral B	PB7
TIOA0	113	PIO A / Peripheral A	PA26
TIOB0	118	PIO C / Peripheral B	PC9
TIOA1	131	PIO A / Peripheral A	PA27
TIOB1	55	PIO C / Peripheral A	PC7
TIOA2	125	PIO A / Peripheral A	PA28
TIOB2	84	PIO C / Peripheral A	PC6

Table 13: TC0, TC1, TC2 Port Pinout

7.13 TC3, TC4, TC5

Signal	DIMM-Pin	PIO Controller	Port Pin
TCLK3	138	PIO B / Peripheral B	PB16
TCLK4	136	PIO B / Peripheral B	PB17
TIOA3	103	PIO B / Peripheral B	PB0
TIOB3	106	PIO B / Peripheral B	PB1
TIOA4	105	PIO B / Peripheral B	PB2
TIOB4	85	PIO B / Peripheral B	PB18
TIOA5	95	PIO B / Peripheral B	PB3
TIOB5	87	PIO B / Peripheral B	PB19

Table 14: TC3, TC4, TC5 Port Pinout

7.14 ADC

Signal	DIMM-Pin	PIO Controller	Port Pin
AD0	128	PIO C	PC0
AD3	120	PIO C	PC3

Table 15: ADC Port Pinout

The port pins are automatically assigned to the ADC when the corresponding channel is enabled. Channels AD1 and AD2 are not available, as the port pins are used on the module.

8 Signal Description

The SO-DIMM connector provides the signals for the embedded peripheral components of the AT91SAM9G20. If not mentioned, the signals are directly connected to the processor. For a description of the processor pin functionality please take a look at the AT91SAM9G20 user's manual.

Caution:

- The processor is a 3.3V device. Input voltages above 3.6V may cause permanent damage to the processor.

8.1 Control Signals

Following sections describe only the pins which have a special purpose or are not directly connected to the processor.

8.1.1 nRESET

The signal nRESET is the reset input / output of the processor. It can be used for system reset generation and signal shaping. An onboard 1kΩ pullup resistor is connected to the nRESET signal. The nRESET signal can be driven with an open collector or open drain driver.

8.1.2 nBOOTMODE

The signal nBOOTMODE is connected to the BMS signal of the processor. When set high the on chip boot mode is selected and the processor starts execution from internal ROM. When set to low the code at 0x10000000 (external memory area 0) is executed. The external memory area 0 selects the onboard NOR flash if ordered with this assembly option.
For normal operation with NAND flash this signal can be left unconnected, as an onboard 1kΩ pullup resistor is connected to the nBOOTMODE signal.
For further information on this signal please consult the AT91SAM9G20 user's manual.

8.1.3 VDDBU

The signal VDDBU is connected to the VDDBU pin of the processor allowing backup supply using a battery or other permanent power supply.
The input has to be connected to a supply voltage between +0.9V and +1.1V. As most batteries have a voltage larger than 1.0V a voltage regulator has to be used. A good choice with a very low quiescent current is the Ricoh R1100D101C.
If no battery should be used, the pin must be connected to a suitable +1.0V supply. The +1.0V signal at pin 122 can be used for VDDBU supply.

8.1.4 WKUP

The signal WKUP is connected to the WKUP input pin of the processor. A low on this pin wakes up the processor from shutdown. An onboard 100kΩ pullup resistor is provided for the WKUP signal. A pushbutton to GND can be connected to this module pin.

8.1.5 SHDN

The signal SHDN is the output of the processor shutdown controller. It allows control of the main power supply and enables processor controlled power off. This signal needs an external pullup to VDDBU with a value larger than 1MΩ.

8.1.6 +1.0V

At pin 122 of the module the +1.0V cpu core voltage is available. This voltage can be used as VDDBU supply if an external battery is not needed.

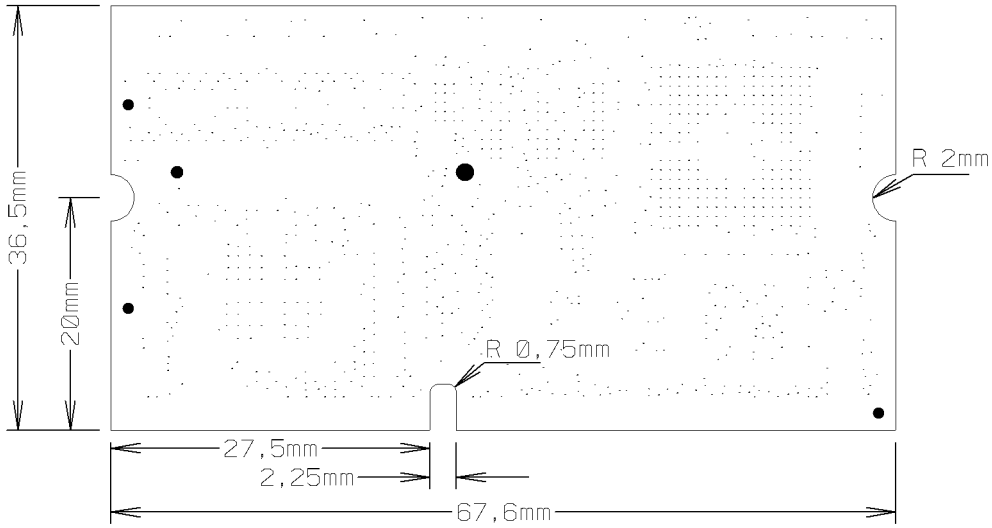
8.1.7 Ethernet Signals

The ethernet interface uses a Micrel KSZ8041 physical layer chip for interfacing to the external RJ45 connector. The termination network for the RX- and TX-signals are already placed on the DIMM-SAM9G20.
The RX signals are available at pins 141 (ETH_RX+) and 143 (ETH-RX-).
The TX signals are available at pins 142 (ETH_TX+) and 144 (ETH-TX-).
The analog center voltage is available at pins 139 and 140 (ETH_VDDA).
Due to the size of the recommended components, the decoupling of the analog pin ETH_VDDA needs additional external components for good ripple rejection. 10µF ceramic or tantalum capacitors should be mounted as close as possible to the SO-DIMM connector pins.

All other DIMM-SAM9G20 signal pins are directly connected to the corresponding I/O pin of the processor.

9 Mechanical Dimensions

9.1 DIMM-SAM9G20 Module



Picture 2: Module Dimensions

9.2 DIMM Connector

The DIMM-SAM9G20 uses standard SO-DIMM memory sockets for connection to the carrier board. 3.3V as well as 5V keying can be used for the SO-DIMM sockets, as the DIMM-SAM9G20 features a wide key for both keying types.

Caution:

- The pinout of the DIMM-SAM9G20 SO-DIMM connector is NOT compatible with memory sockets.
  Insertion into a socket with wrong pinout may damage the DIMM-SAM9G20 and the carrier board!

Following table is a short list of possible DIMM connectors which can be used with the DIMM-SAM9G20. Most connectors are right angled connectors with varying height.

Manufacturer	Order Code	Description
AMP/Tyco	390112-1	Horizontal mounted, SMD, low profile
AMP/Tyco	390322-1	Horizontal mounted, SMD, high profile
Molex	54698-7000	Horizontal mounted, SMD, low profile

Table 16: DIMM Socket Selection

10 Installing the DIMM-SAM9G20

10.1 Installing the module

Caution:

- Always wear a grounded wrist strap when handling the DIMM-SAM9G20 in order to discharge any static electricity from your body!
- Always unplug your system from power before installing the DIMM-SAM9G20.

The DIMM-SAM9G20 does not require any configurations before installation. Perform the following step-by-step instructions to install the DIMM-SAM9G20 in your system:

- **Unplug your system from the power outlet.**
- Insert the DIMM-SAM9G20 into the SO-DIMM connector on the carrier board. The module should drop easily into place. Do not force the module into the socket to avoid damage to the socket. If the module does not fit check its alignment. You also may pull the two locking clips gently sideways away form the socket during insertion before the module is locked into the socket.
- Reconnect your system to the power outlet. The DIMM-SAM9G20 is ready to use now.

11 Technical Specifications

Microcontroller

CPU type:	ATMEl AT91SAM9G20 ARM920T microcontroller
CPU speed:	400 MHz

Memory

SDRAM:	64 MByte, optional 128 MByte, 32-bit data bus
NAND-Flash:	64 MByte, larger devices on request

External power supply

Main Supply:	3.3 V ± 5 %, 300 mA max.
Input connection:	SO-DIMM pins +3.3V and GND
Backup Supply:	1.0V ± 0.1V, 50µA max.

On board power regulator

Type:	Low drop out linear voltage regulator
Output:	1.0 V, 150 mA max.
Output connection:	SO-DIMM pin +1.0V, max 20mW

General information

Connector:	SO-DIMM card edge, 144 pins
Power consumption:	3.3 V, 220 mA typical
PCB type:	8 layer lead free SO-DIMM module
Operating temperature:	-25 °C to +85 °C
Storage temperature:	-25 °C to +85 °C
Humidity:	10 - 90 %, non condensing
Dimensions (d x w x h):	36.5 x 67.6 x 2.5 mm
Weight:	30 g

12 Important Documents

12.1 Atmel AT91SAM9G20 Datasheet

Literatur Number: 6384E.pdf
Revision History: E
Publication Date: 05-Feb-2010
www.atmel.com

12.2 Micrel KSZ8043INL Datasheet

Revision: 1.2
Publication Date: Jul-2008
www.micrel.com

12.3 Samsung K9F1208X0C Datasheet

Revision: 1.1
Publication Date: 18-Jun-2007
http://www.samsung.com/Products/Semiconductor/

12.4 Numonyx P33 Flash Memory Datasheet

Order Number: 208034-03
Publication Date: July-2010
http://www.numonyx.com

12.5 ESMT M12L2561616A Datasheet

Revision: 1.2
Publication Date: May-2008
http://www.esmt.com.tw

13 Hardware Revision History

Version	Date	Alteration
1.0	18.11.10	Prototype
1.1	10.04.11	1st Official Release

14 Document Revision History

Version	Date	Alteration
1.0	13.05.11	Initial Draft